



**128Mb MULTIBANK BURST FLASH
32Mb/64Mb ASYNC/PAGE CellularRAM COMBO**

**FLASH AND CellularRAM™
COMBO MEMORY**

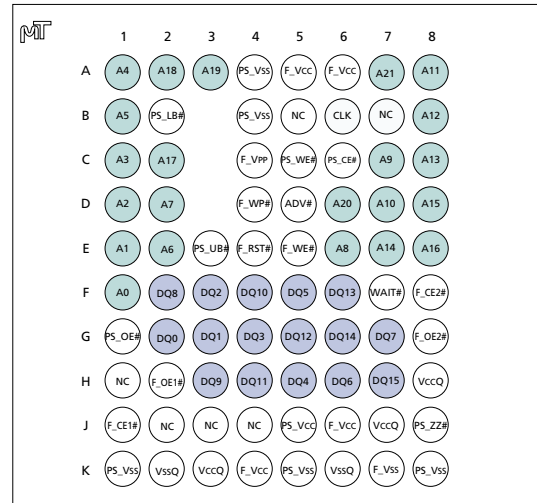
**MT28C128532W18/W30D
MT28C128564W18/W30D**

Low Voltage, Wireless Temperature

Features

- Stacked die Combo package
Includes two 64Mb Flash devices
Choice of either one 32Mb or one 64Mb CellularRAM™ device
- Basic configuration
Flash
Flexible multibank architecture
4 Meg x 16 Async/Page/Burst interface
Support for true concurrent operations with no latency
CellularRAM
Low-power, high-density design
2 Meg x 16 or 4 Meg x 16 configurations
Async/Page
- F_VCC, VCCQ, F_VPP, PS_VCC voltages
1.70V (MIN)/1.95V (MAX) F_VCC, PS_VCC
1.70V (MIN)/2.24V (MAX) VCCQ (W18)
1.70V (MIN)/3.3V(MAX) VCCQ (W30)
1.80V (TYP) F_VPP (in-system PROGRAM/ERASE)
12V ±5% (HV) F_VPP (in-house programming and accelerated programming algorithm [APA] activation)
- Asynchronous access time
Flash/CellularRAM access time: 60ns @ 1.70V VCC
- Page Mode read access (W18/W30)
Interpage read access: 60ns @ 1.70V F_VCC, PS_VCC (W18)
Intrapage read access: 20ns @ 1.70V F_VCC, PS_VCC (W18)
Interpage read access: 70ns @ 1.70V F_VCC, PS_VCC (W30)
Intrapage read access: 22ns @ 1.70V F_VCC, PS_VCC (W30)
- Enhanced suspend options
ERASE-SUSPEND-to-READ within same bank
PROGRAM-SUSPEND-to-READ within same bank
ERASE-SUSPEND-to-PROGRAM within same bank
- Read/Write CellularRAM during program/erase of Flash
- Each Flash contains two 64-bit chip protection registers for security purposes
- Flash PROGRAM/ERASE cycles
100,000 WRITE/ERASE cycles per block
- Cross-compatible command set support
Extended command set
Common Flash interface (CFI) compliant
- Manufacturer's ID (ManID)
Micron® (0x2Ch)
Intel® (0x89h)

Figure 1: 77-Ball FBGA



Top View
(Ball Down)

Options

- Timing
60ns
70ns
- Burst Frequency
66 MHz¹
54 MHz
- Boot Block Configuration
Top/Top TT
Top/Bottom TB
Bottom/Top BT
Bottom/Bottom BB
- I/O Voltage Range
VCCQ 1.70V–1.95V 18
VCCQ 1.70V–3.3V 30
- Manufacturer's ID (ManID)
Micron (0x2Ch) None
Intel (0x89h) K
- Operating Temperature Range
Wireless Temperature (-25°C to +85°C) WT
- Package
77-ball FBGA (8 x 10 grid) FW

Marking

NOTE: 1. Contact factory for availability.

Part Number Example:

MT28C128564W18DFW-705 BBWT



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General Description

The MT28C128532W18/W30D and MT28C128564W18/W30D combination Flash and CellularRAM are high-performance, high-density, memory solutions that can significantly improve system performance. The Flash architecture features a multi-partition configuration that supports READ-while-PROGRAM/ERASE operations with no latency. A 4Mb partition size enables optimal design flexibility.

Two Flash devices are stacked to achieve the 128Mb density. Each Flash die has a dedicated CE# and OE# control, enabling each Flash to be independently selectable.

The MT28C128532W18/W30D and MT28C128564W18/W30D stacked Flash devices enable soft protection for blocks, as read only, by configuring soft protection registers with dedicated command sequences. For security purposes, two user-programmable 64-bit chip protection registers are provided for each Flash device.

The embedded WORD PROGRAM and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). An on-chip device status register can be used to monitor the WSM status and determine the progress of the PROGRAM/ERASE tasks.

Each Flash device has a read configuration register (RCR) that defines how the Flash interacts with the memory bus. For device specifications and additional documentation concerning Flash and CellularRAM features, please refer to the MT28F644W18/W30 data sheet at www.micron.com/flash and the MT45W2MW16PFA and MT45W4MW16PFA data sheets at <http://www.micron.com/cellularram>.

The CellularRAM architecture features high-speed CMOS, dynamic random-access memories developed for low-power portable applications. The CellularRAM device is available in either 32Mb or 64Mb densities.

To operate seamlessly on a burst Flash bus, CellularRAM products have incorporated a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

The refresh configuration register (CR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time during normal operation. Special attention has been focused on standby current consumption during self-refresh.

CellularRAM products include three system-accessible mechanisms used to minimize standby current. Partial array refresh (PAR) limits refresh to the portion of the memory array being used. Temperature compensated refresh (TCR) is used to adjust the refresh rate according to the ambient temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Deep power down (DPD) halts the REFRESH operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are adjusted through the CR.

Please refer to Micron's Web site www.micron.com/flash for the latest MT28F644W18/W30 Flash data sheet and <http://www.micron.com/cellularram> for the latest MT45W2MW16PFA and MT45W4MW16PFA CellularRAM data sheet.

Flash Configurations

Each Flash memory implements a multibank architecture (16 banks of 4Mb each) to allow concurrent operations. Any address within a block address range selects that block for the required READ, PROGRAM, or ERASE operation.

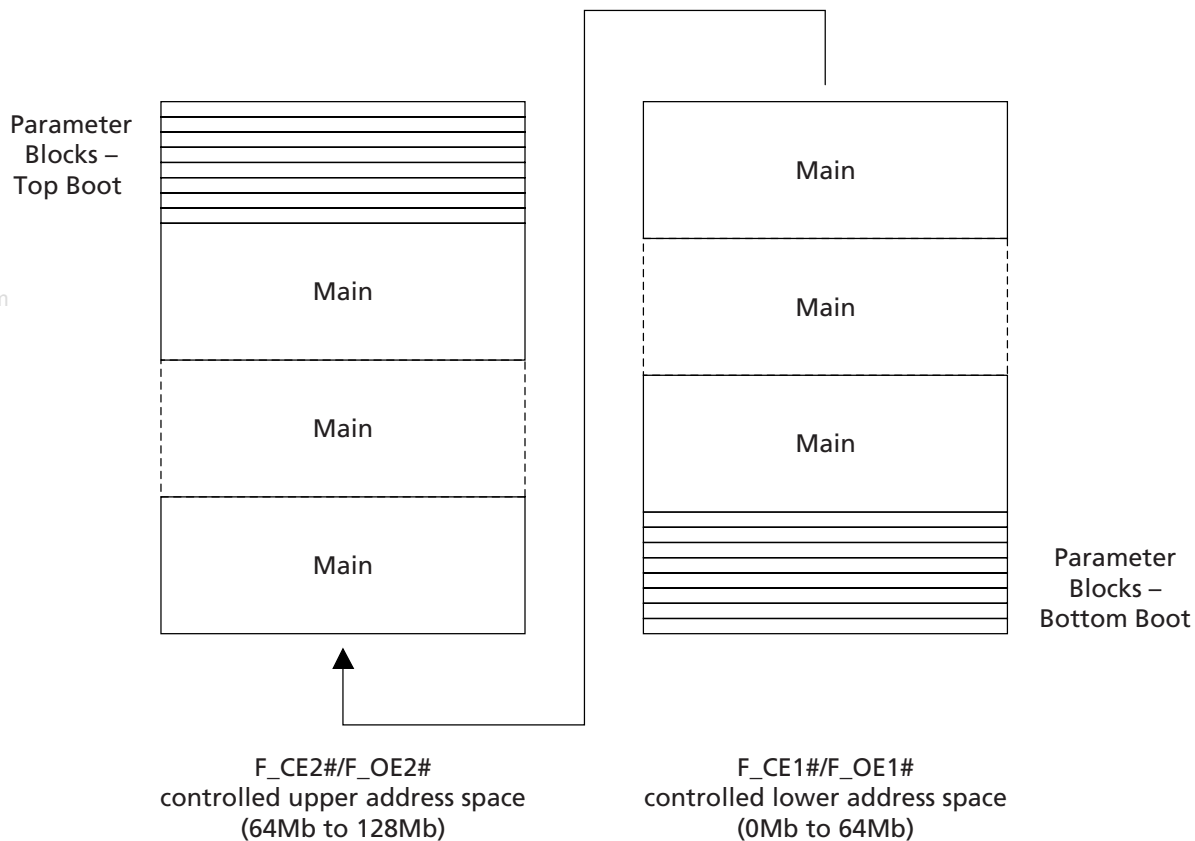
Each Flash memory features eight 4K-word sectors (8 x 65,536 bits), designated as parameter blocks, and the remaining part is organized in main blocks of 32K words each (524,288 bits). The parameter blocks are addressed either by the low order addresses (bottom boot) or by the higher order addresses (top boot).

The two Flash devices can be supplied with any combination of top or bottom boot (e.g., top/top, bottom/bottom, top/bottom, or bottom/top). Please see Figures 2 and 3 for more information.



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Figure 2: Flash Memory Map

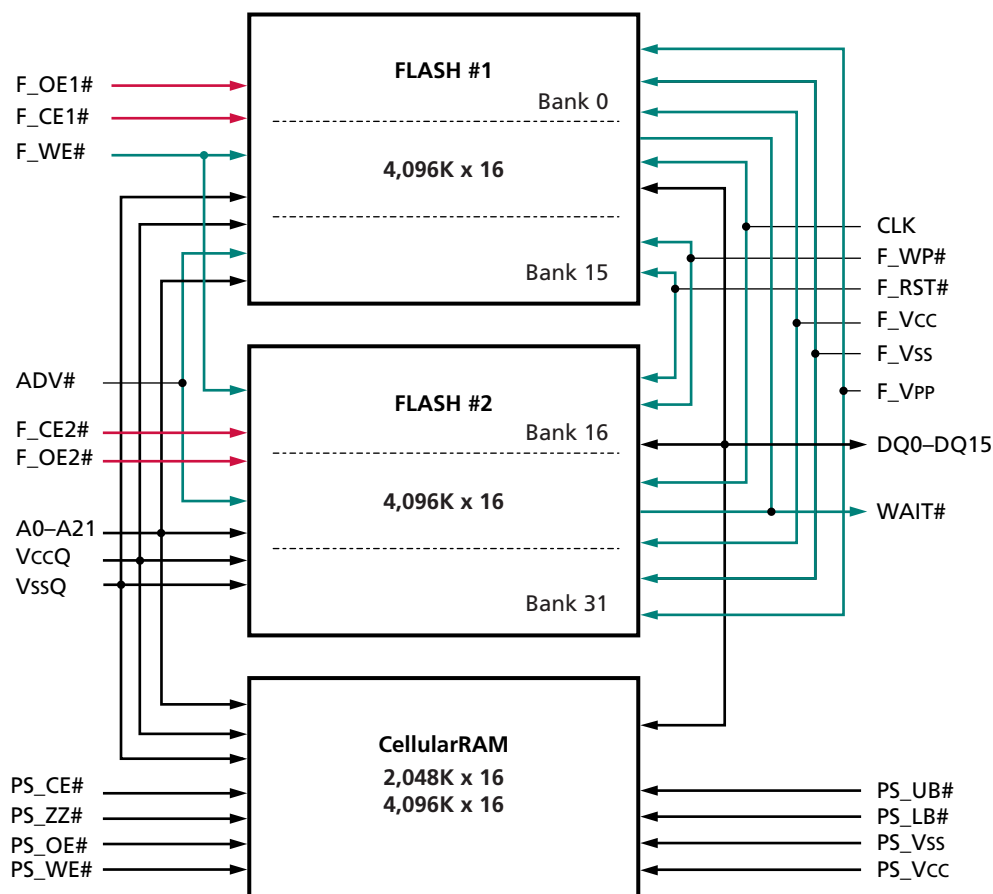


NOTE:
Figure 2 shows a BT (bottom/top) dual Flash configuration.



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Figure 3: Block Diagram



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Device Marking

Due to the size of the package, the Micron® standard part number is not printed on the top of each device. Instead, an abbreviated device mark com-

prised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers in Table 1.

Table 1: Cross-Reference for Abbreviated Device Marks

PRODUCT PART NUMBER	PRODUCT MARKING	SAMPLE MARKING	MECHANICAL MARKING
MT28C128532W18DFW-606 BTWT	FW625	FX625	FY625
MT28C128532W18DFW-606 BBWT	FW631	FX631	FY631
MT28C128532W18DFW-705 BTWT	FW632	FX632	FY632
MT28C128532W18DFW-705 TTWT	FW626	FX626	FY626
MT28C128564W18DFW-606 BTWT	FW627	FX627	FY627
MT28C128564W18DFW-705 BTWT	FW637	FX637	FY637
MT28C128532W18DFW-606 TBWT	FW639	FX639	FY639
MT28C128532W18DFW-606 BBWT	FW642	FX642	FY642
MT28C128532W18DFW-705 BBWT	FW638	FX638	FY638
MT28C128532W18DFW-705 TTWT	FW643	FX643	FY643
MT28C128532W30DFW-606 BBWT	FW649	FX649	FY649
MT28C128532W30DFW-705 TBWT	FW651	FX651	FY651
MT28C128564W30DFW-606 BTWT	FW650	FX650	FY650
MT28C128564W30DFW-705 BTWT	FW640	FX640	FY640



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Part Numbering Information

Micron's low-power devices are available with several different combinations of features (see Figure 4).

Valid combinations of features and their corresponding part numbers are listed in Table 2.

Figure 4: Part Number Chart

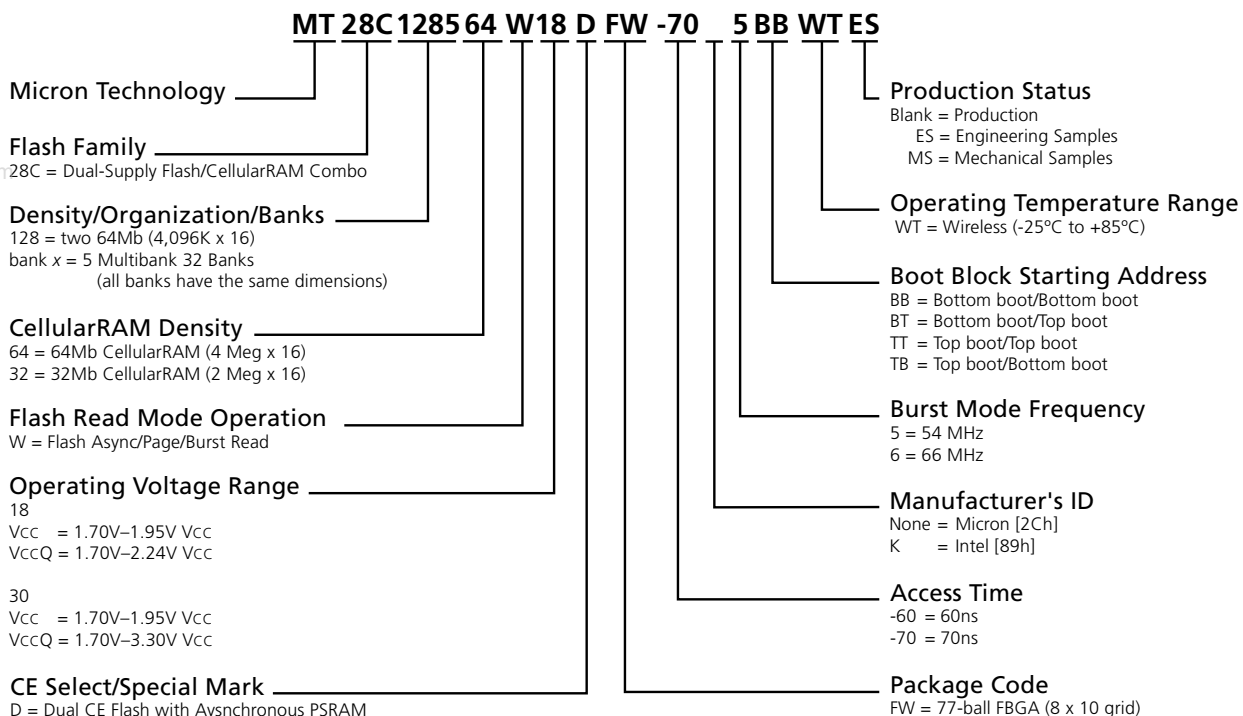


Table 2: Valid Part Number Combinations

PART NUMBER	ManID	ACCESS TIME (ns)	BOOT BLOCK STARTING ADDRESS	BURST FREQUENCY (MHz)
MT28C128532W18DFW-606 BTWT	Micron	-60	Bottom/Top	66
MT28C128532W18DFW-606 BBWT	Micron	-60	Bottom/Bottom	66
MT28C128532W18DFW-705 BTWT	Micron	-70	Bottom/Top	54
MT28C128532W18DFW-705 TTWT	Micron	-70	Top/Top	54
MT28C128564W18DFW-606 BTWT	Micron	-60	Bottom/Top	66
MT28C128564W18DFW-705 BTWT	Micron	-70	Bottom/Top	54
MT28C128532W18DFW-606 TBWT	Micron	-60	Top/Bottom	66
MT28C128532W18DFW-606 BBWT	Micron	-60	Bottom/Bottom	66
MT28C128532W18DFW-705 BBWT	Micron	-70	Bottom/Bottom	54
MT28C128532W18DFW-705 TTWT	Micron	-70	Top/Top	54
MT28C128532W30DFW-606 BBWT	Micron	-60	Bottom/Bottom	66
MT28C128532W30DFW-705 TBWT	Micron	-70	Top/Bottom	54
MT28C128564W30DFW-606 BTWT	Micron	-60	Bottom/Top	66
MT28C128564W30DFW-705 BTWT	Micron	-70	Bottom/Top	54



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Table 3: Ball Descriptions

77-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTIONS
F1, E1, D1, C1, A1, B1, E2, D2, E6, C7, D7, A8, B8, C8, E7, D8, E8, C2, A2, A3, D6, A7	A0–A21	Input	Addresses: Flash: A0–A21 (128Mb “D”) CellularRAM: A0–A20 (32Mb) CellularRAM: A0–A21 (64Mb)
J1	F_CE1#	Input	Flash Chip Enable #1
F8	F_CE2#	Input	Flash Chip Enable #2
H2	F_OE1#	Input	Flash Output Enable #1
G8	F_OE2#	Input	Flash Output Enable #2
E5	F_WE#	Input	Flash Write Enable
D4	F_WP#	Input	Flash Write Protect
B2	PS_LB#	Input	CellularRAM Lower Byte Control
E3	PS_UB#	Input	CellularRAM Upper Byte Control
C5	PS_WE#	Input	CellularRAM Write Enable
G1	PS_OE#	Input	CellularRAM Output Enable
C6	PS_CE#	Input	CellularRAM Chip Enable
J8	PS_ZZ#	Input	CellularRAM Deep Sleep Mode and Configuration Mode
D5	ADV#	Input	Flash Address Valid (Burst operation only)
B6	CLK	Input	Flash Clock (Burst operation only)
E4	F_RST#	Input	Flash Reset
G2, G3, F3, G4, H5, F5, H6, G7, F2, H3, F4, H4, G5, F6, G6, H7	DQ0–DQ15	I/O	Flash/CellularRAM Data Input/Output
F7	WAIT#	Output	Flash WAIT#
K7	F_Vss	Supply	Flash Core Ground
C4	F_VPP	Supply	Flash VPP
J6	F_Vcc	Supply	Flash Core Power Supply
K5	PS_Vss	Supply	CellularRAM Core Ground
J5	PS_Vcc	Supply	CellularRAM Core Power Supply
J7	VccQ	Supply	Flash/CellularRAM I/O Supply
K6	VssQ	Supply	Flash/CellularRAM I/O Ground
B5, B7, H1, J2, J3, J4	NC	–	No Connect
B3, C3, D3	–	–	Ball not Mounted



Boot Configurations

The possible configurations for Flash die are shown in Table 4 below. This table shows the possible configurations of the two Flash devices for either top boot or bottom boot: F_CE1# and F_CE2# indicate to which Flash die the configuration is referred.

Table 4: Possible Boot Configurations for Flash Die

CONFIGURATION	F_CE1#	F_CE2#	ORDER CODE
Top/Top	Top	Top	TT
Bottom/Top	Bottom	Top	BT
Top/Bottom	Top	Bottom	TB
Bottom/Bottom	Bottom	Bottom	BB

MultiChip Packaging Considerations

Multichip packaging presents unique challenges when controlling complex memory devices.

The MT28C128532W18/W30D and MT28C128564W18/W30D devices combine two Micron Flash devices with a single CellularRAM device.

Unique IDs, State Machines, and Registers

Each Flash device has a separate command state machine (CSM) and status register (SR) and read configuration register (RCR). The RCR settings are separate and can be different for the upper and lower device. Each Flash device has its own OTP, CFI, and device code. Depending on the boot configuration of each Flash device, the OTP, CFI, and device code information may differ.

Both Flash devices will share the same ManID, either Micron (0x2Ch) or Intel (0x89h), which is defined by the part number. (See Figure 4 on page 9.)

The CellularRAM has a configuration register (CR) that defines how the device performs self refresh.

Command Codes

All Flash command codes are independent within each device. Care must be taken when crossing the array boundary between the upper and lower Flash and the CellularRAM to ensure that only one device is enabled at one time.

In a two-cycle command sequence such as word program (0x40/data), it is required that both commands be issued to the same device.

It is not recommended that READ and ERASE operations occur simultaneously on two devices.

READ Operation

Page and burst read modes are limited to the address boundaries of each device. A new page/ burst operation must be started when crossing a device boundary.

Flash Reset

The reset control is shared by both Flash die. Bringing RST# control LOW will reset both the upper and lower device.

Power Consumption

Multiple chip packaging requires that power calculations consider the active operation of the upper and lower Flash as well as that of the CellularRAM. Total power consumed will be the sum of the currents associated with the state of each device. Table 9 on page 14 shows the power consumption specifications.

Table 5: Truth Table

	MODES	FLASH SIGNALS					SHARED SIGNALS			CellularRAM SIGNALS					MEMORY OUTPUT	
		F_CE1#	F_CE2#	F_OE1#	F_OE2#	F_WE#	F_RP#	ADV#	WAIT#	PS_CE#	PS_ZZ#	PS_OE#	PS_UB/LB	PS_WE#	MEMORY BUS CONTROL	DQ0-DQ15
FLASH F_CE1#	Read	L	H	L	H	H	H	L	Valid	CellularRAM must be in High-Z					Flash	DOUT
	Write	L	H	H	H	L	H	L	Valid	CellularRAM must be in High-Z					Flash	DIN
	Standby	H	X	X	X	X	H	X	X	CellularRAM any mode allowable					Other	High-Z
	Output Disable	L	X	H	X	H	H	X	X	CellularRAM any mode allowable					Other	High-Z
	Reset	X	X	X	X	X	L	X	X	CellularRAM any mode allowable					None	High-Z
FLASH F_CE2#	Read	H	L	H	L	H	H	L	Valid	CellularRAM must be in High-Z					Flash	DOUT
	Write	H	L	H	H	L	H	L	Valid	CellularRAM must be in High-Z					Flash	DIN
	Standby	X	H	X	X	X	H	X	X	CellularRAM any mode allowable					Other	High-Z
	Output Disable	X	L	X	H	H	H	X	X	CellularRAM any mode allowable					Other	High-Z
	Reset	X	X	X	X	X	L	X	X	CellularRAM any mode allowable					None	High-Z
CellularRAM	Read	Flash must be in High-Z					X	L	Valid	L	H	L	L	H	PSRAM	DOUT
	Write	Flash must be in High-Z					X	L	Valid	L	H	H	L	L	PSRAM	DIN
	Standby	Flash any mode allowable					X	X	X	H	H	X	X	X	Other	High-Z
	Output Disable	Flash any mode allowable					X	X	X	L	H	H	X	X	Other	High-Z
	Deep Sleep Mode	Flash any mode allowable					X	X	X	H	L	X	X	X	Other	High-Z



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Flash Electrical Specifications

Table 6: Absolute Maximum Ratings

Note 1

PARAMETERS/CONDITIONS		MIN	MAX	UNITS	NOTES
Voltage to any ball except Vcc, VccQ, and Vpp	W18 W30	-0.5 -0.5	+2.45 +3.45	V	
Vpp Voltage		-0.2	+14	V	2
Vcc Supply Voltage	W18 W30	-0.2	+2.45 +2.5	V	
VccQ Supply Voltage	W18 W30	-0.2	+2.45 +3.3465	V	
Output Short Circuit Current			100	mA	
Operating Temperature Range		-25	+85	°C	
Storage Temperature Range		-55	+125	°C	
Soldering Cycle			+260°C for 10s		

NOTE:

- Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Maximum DC voltage on Vpp may overshoot to +14V for periods <20ns.

Table 7: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Temperature	T _A	-25	–	+85	°C
Vcc Supply Voltage	Vcc	1.70	–	1.95	V
I/O Supply Voltage	VccQ (W18)	1.70	–	2.24	V
	VccQ (W30)			3.3	
Input/Output Capacitance: DQs	C _{IO}	–	4.0	6.5	pF
Vpp Voltage	Vpp1	0.9	–	1.95	V
Vpp In-factory Programming Voltage	Vpp2	11.4	–	12.6	V
Block Erase Cycling (Vpp = Vpp1)		–	–	100,000	Cycles
Block Erase Cycling (Vpp = Vpp2)		–	–	1,000	Cycles
Time for Vpp at Vpp2	t _{PPH}	–	–	100	Hours

Table 8: Capacitance

T_A = +25°C; f = 1 MHz

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C _{IN}	TBD	TBD	pF
Output Capacitance	C _{OUT}	TBD	TBD	pF



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Table 9: DC Characteristics

Notes appear on following page; all currents are in RMS unless otherwise noted

PARAMETER	SYM	MIN	W18/W30		UNITS	NOTES
			TYP	MAX		
Input Low Voltage	V _{IL}	0		0.4	V	1
Input High Voltage	V _{IH}	V _{CCQ} - 0.4		V _{CCQ}	V	1
Output Low Voltage I _{OL} = 100μA	V _{OL}			0.1	V	
Output High Voltage I _{OH} = -100μA	V _{OH}	V _{CCQ} - 0.1			V	
V _{PP} Lockout Voltage	F_VPPLK	0.4			V	
V _{CC} Lock	F_VLKO	1.0			V	
V _{CCQ} Lock	F_VILKOQ	TBD			V	
Input Load Current	F_ILI			±1	μA	
Output Leakage Current	F_ILO			±1	μA	
V _{CC} Standby Current with 32Mb PSRAM with 64Mb PSRAM	I _{CCS}			140 150	μA	
Asynchronous Read Current	F_ICCR		2	4	mA	
Page Read Current	F_ICCR		3	6	mA	
V _{CC} Burst Read Current 4-word Burst Read Current @ 54 MHz 4-word Burst Read Current @ 66 MHz	F_ICCR		3 3	5 5	mA	2, 3, 5
V _{CC} Burst Read Current 8-word Burst Read Current @ 54 MHz 8-word Burst Read Current @ 66 MHz	F_ICCR		3 3	5 5	mA	2, 3, 5
V _{CC} Continuous Burst Read Current Continous Burst Read Current @ 54 MHz Continous Burst Read Current @ 66 MHz	F_ICCR		7 8	10 12	mA	2, 3, 5
F_V _{CC} Program Current F_V _{PP} = F_V _{PP1} , Program in Progress F_V _{PP} = F_V _{PP2} , Program in Progress	F_ICCW		18 8	25 15	mA	
F_V _{CC} Block Erase Current F_V _{PP} = F_V _{PP1} , Block Erase in Progress F_V _{PP} = F_V _{PP2} , Block Erase in Progress	F_ICCE		18 8	30 15	mA	
F_V _{CC} Program Suspend Current	F_ICCWS		7	25	μA	4
F_V _{CC} Erase Suspend Current	F_ICCES		7	25	μA	4
F_V _{CC} Automatic Power Save Current	F_ICCAPS		7	25	μA	
F_V _{PP} Standby Current	F_IPPS		0.2	5	μA	
F_V _{PP} Program Suspend Current	F_IPPWS		0.2	5	μA	
F_V _{PP} Erase Suspend Current	F_IPPES		0.2	5	μA	
F_V _{PP} Read Current	F_IPPR		2	15	μA	



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Table 9: DC Characteristics (continued)

Notes appear on following page; all currents are in RMS unless otherwise noted

PARAMETER	SYM	MIN	W18/W30		UNITS	NOTES
			TYP	MAX		
F_VPP Program Current F_VPP = F_VPP1, Program in Progress F_VPP = F_VPP2, Program in Progress	F_IPPW		0.05 8	0.10 22	mA	
F_VPP Erase Current F_VPP = F_VPP1, Erase in Progress F_VPP = F_VPP2, Erase in Progress	F_IPPE		0.05 8	0.10 22	mA	
Read Operating Current Asynchronous Random READ Asynchronous Page READ Initial Access, Burst READ Continuous Burst READ	PS_Icc1			(-60) 25 15 35 15 (-70) 21 13 21 11	mA	6, 7, 8
Write Operating Current	PS_Icc2 (-60) (-70)			25 21	mA	6, 7, 9

NOTE:

1. V_{IL} may decrease to $-0.4V$ and V_{IH} may increase to $V_{CCQ} + 0.3V$ for durations not to exceed 20ns.
2. APS mode reduces I_{CC} to approximately I_{CCS} levels.
3. Test conditions: $V_{CC} = V_{CC} (MAX)$, $CE\# = V_{IL}$, $OE\# = V_{IH}$. All other inputs = V_{IH} or V_{IL} .
4. I_{CCES} and I_{CCWS} values are valid when the device is deselected. Any READ operation performed while in suspend mode will have an additional current draw of suspend current (I_{CCES} or I_{CCWS}).
5. Synchronous clock = 54 MHz/burst length = continuous is worst case for V_{CC} burst read current.
6. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
7. This device assumes a standby mode if the chip is disabled ($CE\#$ HIGH). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling), regardless of the state of $CE\#$, $UB\#$, and $LB\#$. In order to achieve low standby current all inputs must be either V_{CC} or V_{SS} .
8. $V_{IN} = V_{CC}$ or $0V$ Chip Enabled, $I_{OUT} = 0$.
9. $V_{IN} = V_{CC}$ or $0V$ Chip Enabled, $I_{OUT} = 0$.



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Table 10: CFI

OFFSET	DATA	DESCRIPTION
00	2Ch	Manufacturer's Identification Code (ManID) Micron
	89h	Intel
01	44C6h/8864h	Device ID Code (DevID) Top boot block device ID code (Micron / Intel)
	44C7h/8865h	Bottom boot block device ID code (Micron/Intel)
02 – 0F	reserved	Reserved
10, 11	0051, 0052	"QR"
12	0059	"Y"
13, 14	0003, 0000	Primary OEM command set
15, 16	0039, 0000	Address for primary extended table
17, 18	0000, 0000	Alternate OEM command set
19, 1A	0000, 0000	Address for OEM extended table
1B	0017	Vcc MIN for Erase/Write; Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
1C	0019	Vcc MAX for Erase/Write; Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
1D	00B4	Vpp MIN for Erase/Write; Bit 7–bit 4 volts in hex; Bit 3–bit 0 100mV in BCD
1E	00C6	Vpp MAX for Erase/Write; Bit 7–bit 4 Volts in hex; Bit 3–bit 0 100mV in BCD
1F	0004	Typical timeout for single byte/word program, 2 ⁿ μs, 0000 = not supported
20	0000	Typical timeout for maximum size multiple byte/word program, 2 ⁿ μs, 0000 = not supported
21	000A	Typical timeout for individual block erase, 2 ⁿ s, 0000 = not supported
22	0000	Typical timeout for full chip erase, 2 ⁿ s, 0000 = not supported
23	0004	Maximum timeout for single byte/word program, 2 ⁿ μs, 0000 = not supported
24	0000	Maximum timeout for maximum size multiple byte/word program, 2 ⁿ μs, 0000 = not supported
25	0002	Maximum timeout for individual block erase, 2 ⁿ s, 0000 = not supported
26	0000	Maximum timeout for full chip erase, 2 ⁿ s, 0000 = not supported
27	0017	Device size, 2 ⁿ bytes
28	0001	Bus interface x8 = 0, x16 = 1, x32 = 2, x64 = 3
29	0000	Flash device interface description 0000 = async
2A, 2B	0000, 0000	Maximum number of bytes in multibyte program or page, 2 ⁿ
2C	0002	Number of erase block regions within device (4K words and 32K words)
2D, 2E	007E, 0000	Top boot block device erase block region information 1
	0007, 0000	Bottom boot block device erase block region information 1
2F, 30	0000, 0001	Top boot block device erase block region information 1
	0020, 0000	Bottom boot block device erase block region information 1
31, 32	0007, 0000	Top boot block device erase block region information 2
	007E, 0000	Bottom boot block device erase block region information 2
33, 34	0020, 0000	Top boot block device erase block region information 2
	0000, 0001	Bottom boot block device erase block region information 2
35, 36	0000, 0000	Reserved for future erase block region information
37, 38	0000, 0000	Reserved for future erase block region information
39, 3A	0050, 0052	"PR"
3B	0049	"I"
3C	0031	Major version number, ASCII



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Table 10: CFI (continued)

OFFSET	DATA	DESCRIPTION
3D	0033	Minor version number, ASCII
3E	00E6	Optional Feature and Command Support
3F	0003	Bit 0 Chip erase supported no = 0
40	0000	Bit 1 Suspend erase supported = yes = 1
41	0000	Bit 2 Suspend program supported = yes = 1 Bit 3 Chip lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant individual block locking supported = yes = 1 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1 Bit 8 Synchronous read supported = no = 0 Bit 9 Simultaneous operation supported = yes = 1
42	0001	Program supported after erase suspend = yes
43, 44	0003, 0000	Bit 0 block lock status active = yes; Bit 1 block lock down active = yes
45	0018	Vcc supply optimum, 00 = not supported, Bit 7-bit 4 volts in BCD; Bit 3-bit 0 100mV in BCD
46	00C0	Vpp supply optimum, 00 = not supported, Bit 7-bit 4 volts in BCD; Bit 3-bit 0 100mV in BCD
47	0001	Number of protection register fields in JEDEC ID space
48, 49	0080, 0000	Lock bytes LOW address, lock bytes HIGH address
4A, 4B	0003, 0003	2 ⁿ factory programmed bytes, 2 ⁿ user programmable bytes
4C	0004	Page mode read capability
4D	0004	Number of synchronous mode read configuration fields that follow
4E	0001	Synchronous mode read capability configuration 1
4F	0002	Synchronous mode read capability configuration 2
50	0007	Synchronous mode read capability configuration 3
51	0000	Synchronous mode read capability configuration 4
52	Top: 0002 Bot: 0002	Number of device hardware partition regions within the device
53	Top: 000F Bot: 0001	Number of identical partitions within the partition region
54	Top: 0000 Bot: 0000	Number of identical partitions within the partition region
55	Top: 0011 Bot: 0011	Number of identical partitions within the partition region
56	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in program mode
57	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in erase mode
58	Top: 0001 Bot: 0002	Types of erase block regions in this partition region
59	Top: 0007 Bot: 0007	Partition region 1 erase block type 1 information
5A	Top: 0000 Bot: 0000	Partition region 1 erase block type 1 information
5B	Top: 0000 Bot: 0020	Partition region 1 erase block type 1 information
5C	Top: 0001 Bot: 0000	Partition region 1 erase block type 1 information


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Table 10: CFI (continued)

OFFSET	DATA	DESCRIPTION
5D	Top: 0064	Partition 1 (erase block type 1)
	Bot: 0064	
5E	Top: 0000	Partition 1 (erase block type 1)
	Bot: 0000	
5F	Top: 0001	Partition 1 (erase block type 1) bits per cell; internal ECC
	Bot: 0001	
60	Top: 0003	Partition 1 (erase block type 1) page mode and synchronous mode capabilities
	Bot: 0003	
Bot: 61		Partition region 1 erase block type 2 information
	Bot: 0006	
Bot: 62		Partition region 1 erase block type 2 information
	Bot: 0000	
Bot: 63		Partition region 1 erase block type 2 information
	Bot: 0000	
Bot: 64		Partition region 1 erase block type 2 information
	Bot: 0001	
Bot: 65		Partition region 1 (erase block type 2)
	Bot: 0064	
Bot: 66		Partition region 1 (erase block type 2)
	Bot: 0000	
Bot: 67		Partition region 1 (erase block type 2) bits per cell
	Bot: 0001	
Bot: 68		Partition region 1 (erase block type 2) page mode and synchronous mode capabilities
	Bot: 0003	
Top: 61 Bot: 69	Top: 0001	Number of identical partitions within the partition region
	Bot: 000F	
Top: 62 Bot: 6A	Top: 0000	Number of identical partitions within the partition region
	Bot: 0000	
Top: 63 Bot: 6B	Top: 0011	Number of PROGRAM/ERASE operations allowed in a partition
	Bot: 0011	
Top: 64 Bot: 6C	Top: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in program mode
	Bot: 0000	
Top: 65 Bot: 6D	Top: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in erase mode
	Bot: 0000	
Top: 66 Bot: 6E	Top: 0002	Types of erase block regions in this partition region
	Bot: 0001	
Top: 67 Bot: 6F	Top: 0006	Partition region 2 erase block type 1 information
	Bot: 0007	
Top: 68 Bot: 70	Top: 0000	Partition region 2 erase block type 1 information
	Bot: 0000	
Top: 69 Bot: 71	Top: 0000	Partition region 2 erase block type 1 information
	Bot: 0000	
Top: 6A Bot: 72	Top: 0001	Partition region 2 erase block type 1 information
	Bot: 0001	

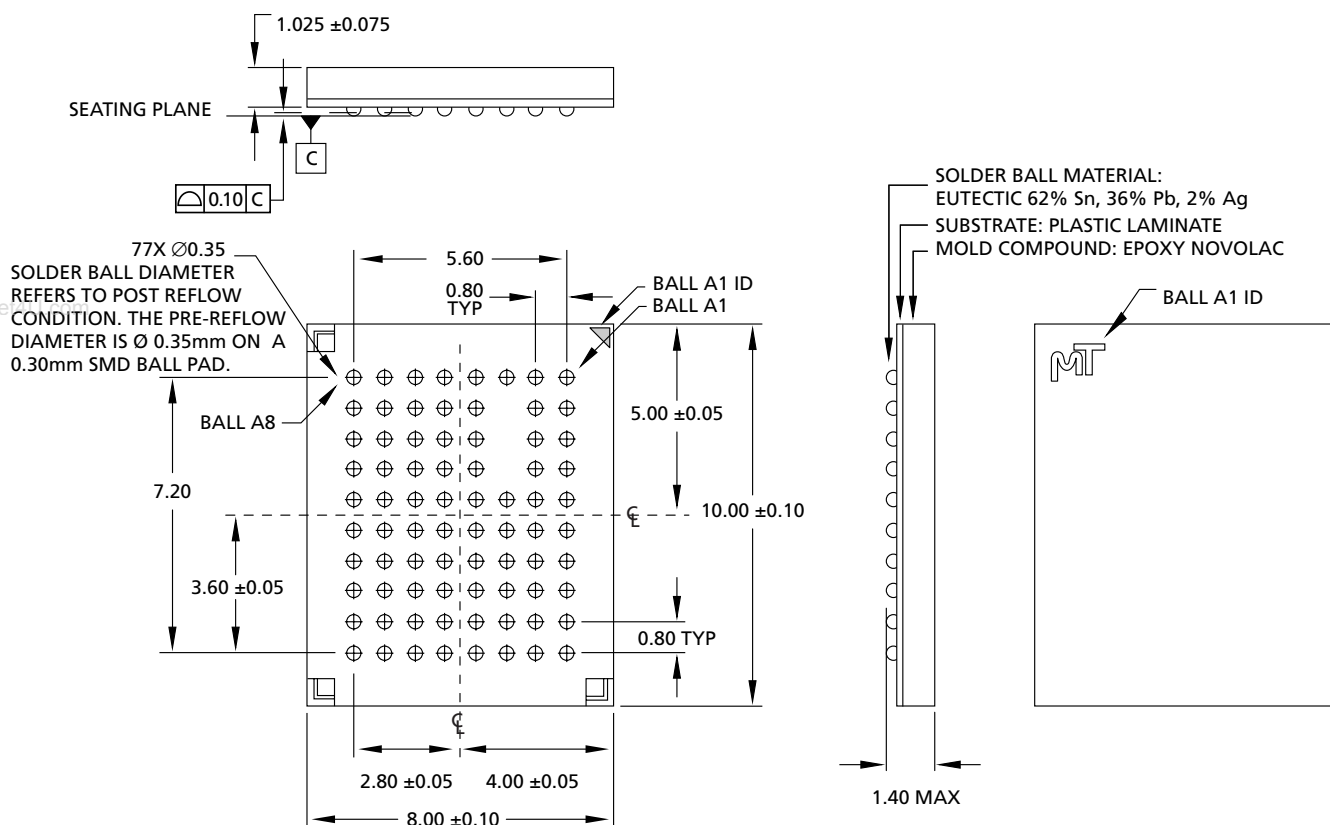

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Table 10: CFI (continued)

OFFSET	DATA	DESCRIPTION
Top: 6B Bot: 73	Top: 0064 Bot: 0064	Partition 2 (erase block type 1)
Top: 6C Bot: 74	Top: 0000 Bot: 0000	Partition 2 (erase block type 1)
Top: 6D Bot: 75	Top: 0001 Bot: 0001	Partition 2 (erase block type 1) bits per cell
Top: 6E Bot: 76	Top: 0003 Bot: 0003	Partition 2 (erase block type 1) page mode and synchronous mode capabilities
Top: 6F	Top: 0007	Partition region 2 erase block type 2 information
Top: 70	Top: 0000	Partition region 2 erase block type 2 information
Top: 71	Top: 0020	Partition region 2 erase block type 2 information
Top: 72	Top: 0000	Partition region 2 erase block type 2 information
Top: 73	Top: 0064	Partition 2 (erase block type 2)
Top: 74	Top: 0000	Partition 2 (erase block type 2)
Top: 75	Top: 0001	Partition 2 (erase block type 2) bits per cell
Top: 76	Top: 0003	Partition 2 (erase block type 2) page mode and synchronous mode capabilities
77		Reserved
78	32Mb: 0020 64Mb: 0040	PSRAM Density
79–7F		Reserved



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Figure 5: 77-Ball FBGA



NOTE:

1. All dimensions in millimeters.

Data Sheet Designation

Advance: This data sheet contains initial descriptions of products still under development.

For additional documentation concerning Flash and CellularRAM features, functional descriptions, programming, and timing, please refer to the MT28F644W18/W30 data sheet at www.micron.com/flash and the MT45W2MW16PFA and MT45W4MW16PFA data sheets at <http://www.micron.com/cellularram>.



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Revision History

Rev B, Advance.....7/03

- Included W30 specification
- Added Intel ManID variant
- Updated mechanical information
- Table 10 (CFI) clarification

Original document, Rev. A.....5/03

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